EL302

DIGITAL INTEGRATED CIRCUITS

LAB #3

CMOS EDGE TRIGGERED D FLIP-FLOP

Due 16.05.2010

İLKER KALYONCU, 10043

2010
Sabanci University

1. INTRODUCTION:

In this project we are going to design a CMOS positive edge triggered master-slave type D flip-flop using AMS 0.35 µm CMOS technology with the following criteria:

- Clock signal parameters: t_{rise} = t_{fall} = 100 ps, duty cycle = 50%, f_{clk} (min) = 1 GHz
- Output load: 50 fF
- Standard cell layout.

Design parameters for AMS 0.35u technology are in Table.2 at the end.

Standard Cell Layout rules are as follows:

- Width (W) and height (H) are multiple of 1.4 µm with W > 2.8 µm
- VDD and GND rails in MET1 layer with H_m = 1.8 µm
- VDD rail with n+ type n-well contact. No DRC errors when cells are merged.
- GND rail with p+ substrate contact. No DRC errors when cells are merged.
- All I/O pads 0.9 x 0.9 μm^2 MET1, center point x and y offsets are multiple of 0.7 µm.
- All cells have an n-well are of same height.

A positive edge, master-slave type D flip-flop is shown on Fig.1. Flip-flop is composed two level triggered latches, called master and slave. Basic principle is that second latch (slave) is driven by the clock signal, while the first one (master) is driven by the inverted version of the clock signal. While master latch is transparent, which occurs when clock is low, slave latch holds its value and while master latch holds its value, which occurs when clock is high, slave latch becomes transparent, thus making the flip-flop sensitive to low-to-high transition of the clock.

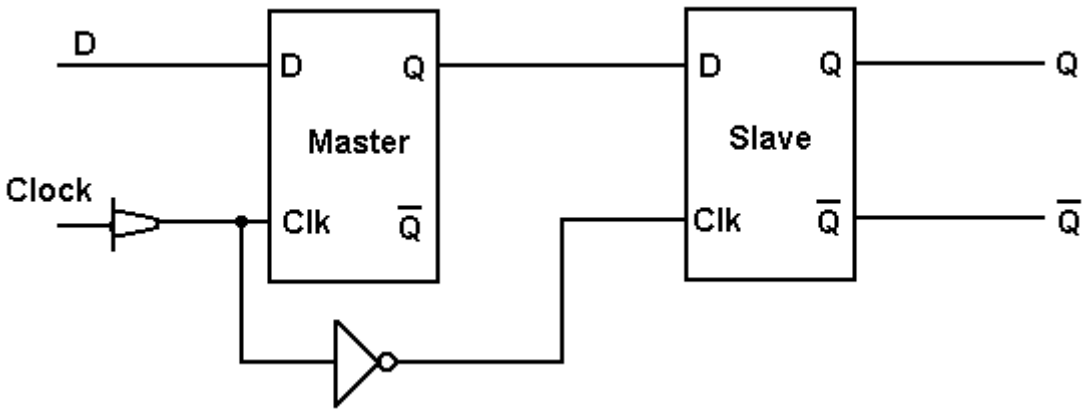
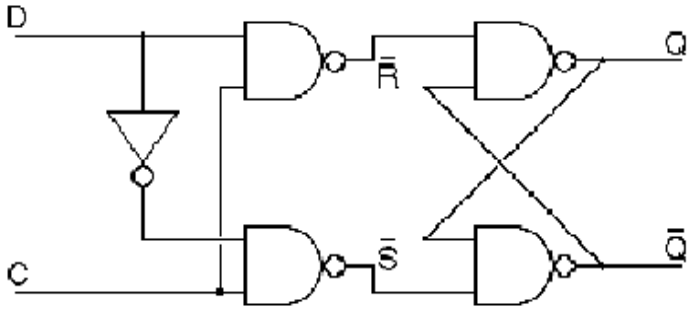


Figure 1: Master-Slave D Flip-Flop

Above figure shows a generic way to implement D Flip-Flop, since we can implement many kinds of D latches, there are many different ways of implementing D flip-flop. On the next part, we are going to investigate different topologies used to implement D flip-flop, and choose which one we are going to use in this design.

2. TOPOLOGY:



C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

Figure 2: NAND2 based D-Latch

Above figure shows a basic implementation of a D-Latch, using NAND2 gates and an inverter. Similarly we can use NOR2 gates as well, to build D-Latch, as can be seen in Fig.3.

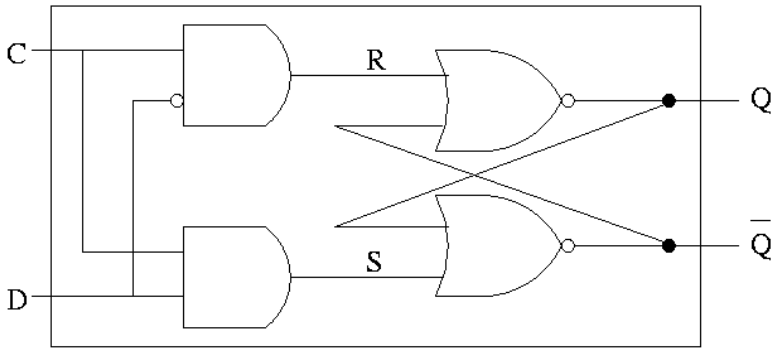


Figure 3: NOR2 and AND2 based D-Latch

However, it is not a wise idea to use AND or NOR gates in our design. Because, in CMOS technology there is no direct implementation of AND gate, thus actually AND gate is nothing but a NAND gate driving an inverter. Also, as can be seen in previous lab reports; propagation, rise and fall times of NOR gate is worse than NAND gate in CMOS technology, as well as NAND implementation has better device dimension ratios between NMOS and PMOS transistors. Thus, we will use NAND2 gates in our D flip-flop design.

Basically we will cascade two level-sensitive NAND2 based D-Latches and drive them with clock signals which are out of phase by 180 degrees. However, there other types of building a D Flip-Flop as follows:

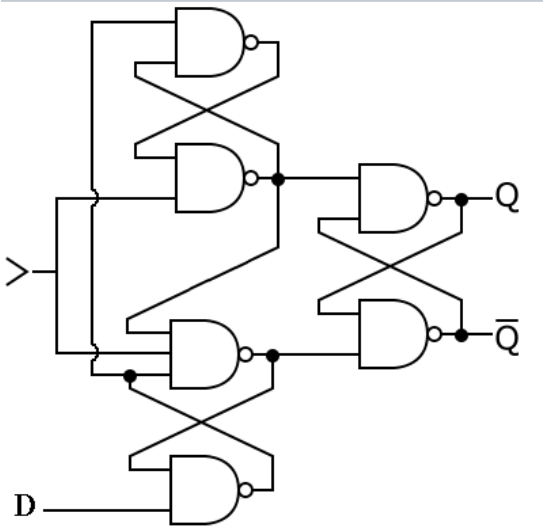


Figure 4: NAND3 based D Flip-Flop

Fig.4 shows an implementation of D Flip-Flop using NAND2 and NAND3 gates. In transistor count, this implementation includes 5x4 (NAND2) + 1x6 (NAND3) = 26 transistors. However, this topology includes a 3 input NAND gate, which will cause extra work to design NAND3 gate. We will not choose this topology, since we previously designed NAND2 gates.

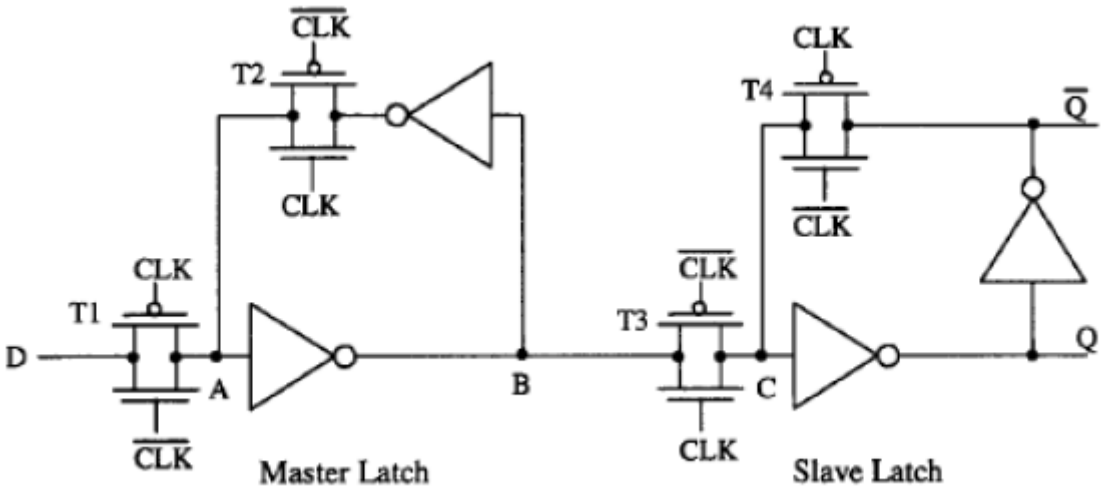


Figure 5: D Flip-Flop with Inverters and Transmission Gates

Transmission gates are very useful to design many sequential circuit components. Fig.5 shows the implementation of D flip-flop with inverters and transmission gates. In transistor count, this topology is very advantages with only 16 transistors used. Transmission gates also help to include asynchronous set and reset functionalities by using NAND2 or NOR2 gates instead of inverters.

However the main drawback of these topologies is that transmission gate is actually a passive component; in other words, it cannot actively drive its output. When transmission gate is on, it is simply a resistor. In CMOS technology, capacitive effect of the load dominates due to gate oxide capacitance, interconnect capacitance and drain to bulk capacitance of the output stage. Thus, the load is always considered as capacitance and since transmission gate is actually a resistor, they form an RC network. The more transmission gates are used, the more RC network is formed and it means more propagation time delays occur in our design. Because of this reason, although the topology in Fig.5 is advantages in terms of transistor count, we will not use it.

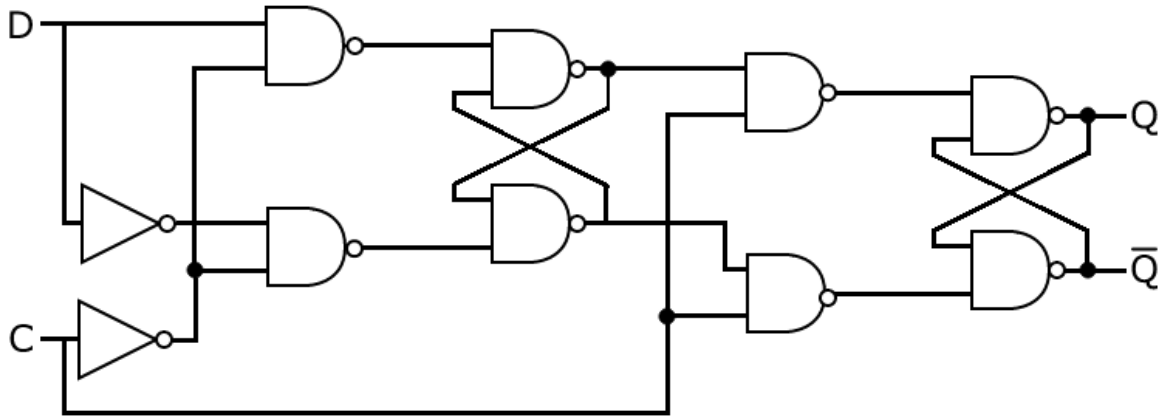


Figure 6: D Flip-Flop based on NAND2 and Inverter

Finally, we will use the topology shown in Fig.6, which is basically two D-Latches cascaded. Total transistor count is slightly large: 8x4 (NAND2) + 2x2 (INV2) = 36. However since only active components are used, smaller propagation delays, rise and fall times are expected. Moreover, in previous labs, we have designed CMOS NAND2 gate and inverter using standard cell layout rules. Thus, it will be very easy to draw layout view of this D flip-flop. This advantage should not be underestimated.

3. DESIGN and HAND CALCULATIONS:

Since NAND2 gates and inverters are used, which we have previously designed, there is no need to make hand calculations for this D flip-flop. After simulations, if results do not meet the requirements (e.g. propagation time delay is so large that flip-flop does not work properly with 1 GHz clock frequency), then we must upgrade our NAND gates and inverters.

Below Fig.7 shows the schematic view of the D flip-flop.

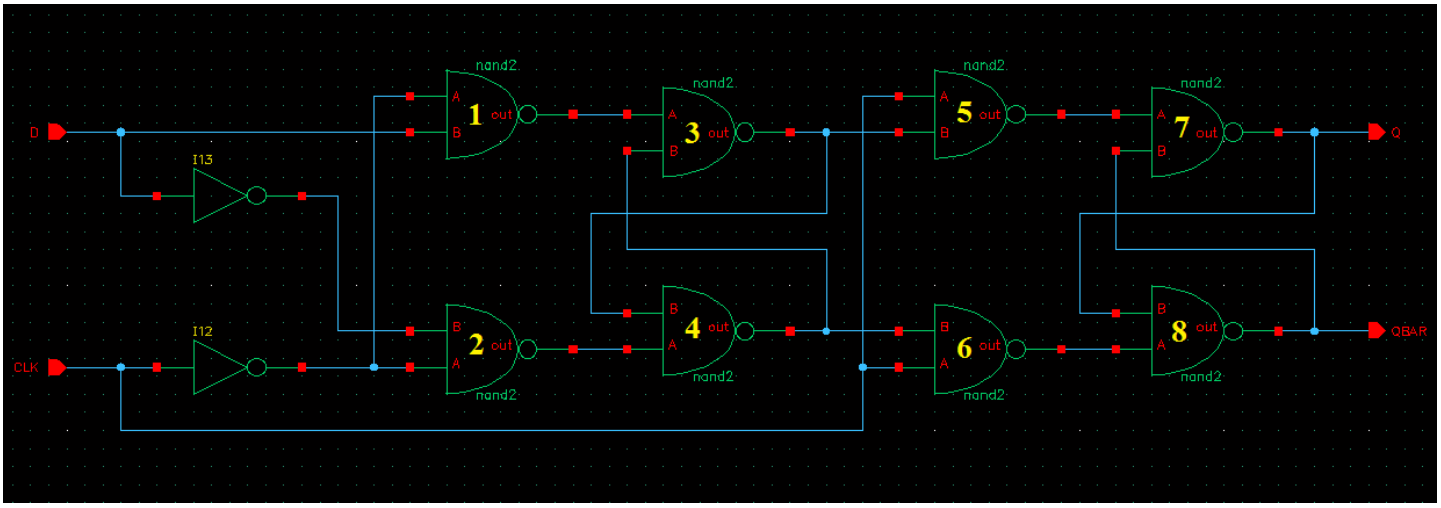


Figure 7: Schematic View of D Flip-Flop

However, there is critical point to be considered in this design to minimize time delays. Our NAND2 gates are not symmetrical! This can be seen in previous lab reports. Thus we should cleverly choose which output to tie to which input. Let us remind that propagation time delays of our NAND gate are worse when transition is triggered by the input B. Thus from now on, we will call input-A faster and input-B slower. So to reduce overall propagation time delay of the flip-flop we should choose input-output relations as follows:

1. D and D' must be tied to faster input of 1st and 2nd NAND gates.
2. Output of 1st and 2nd NAND gates must be tied to faster inputs of the 3rd and 4th NAND gates.
3. When rising edge of the clock comes, 5th and 6th NAND gates should update their output as quick as possible, thus clock signal must be applied to faster inputs of the 5th and 6th NAND gates.
4. Similar to second argument, outputs of 5th and 6th gates must be tied to faster inputs of the 7th and 8th gates.

By making these connections we reduce the overall propagation time delay as much as possible. Also we will use maximum inverters build in previous labs to make the flip flop operate as quickly as possible.

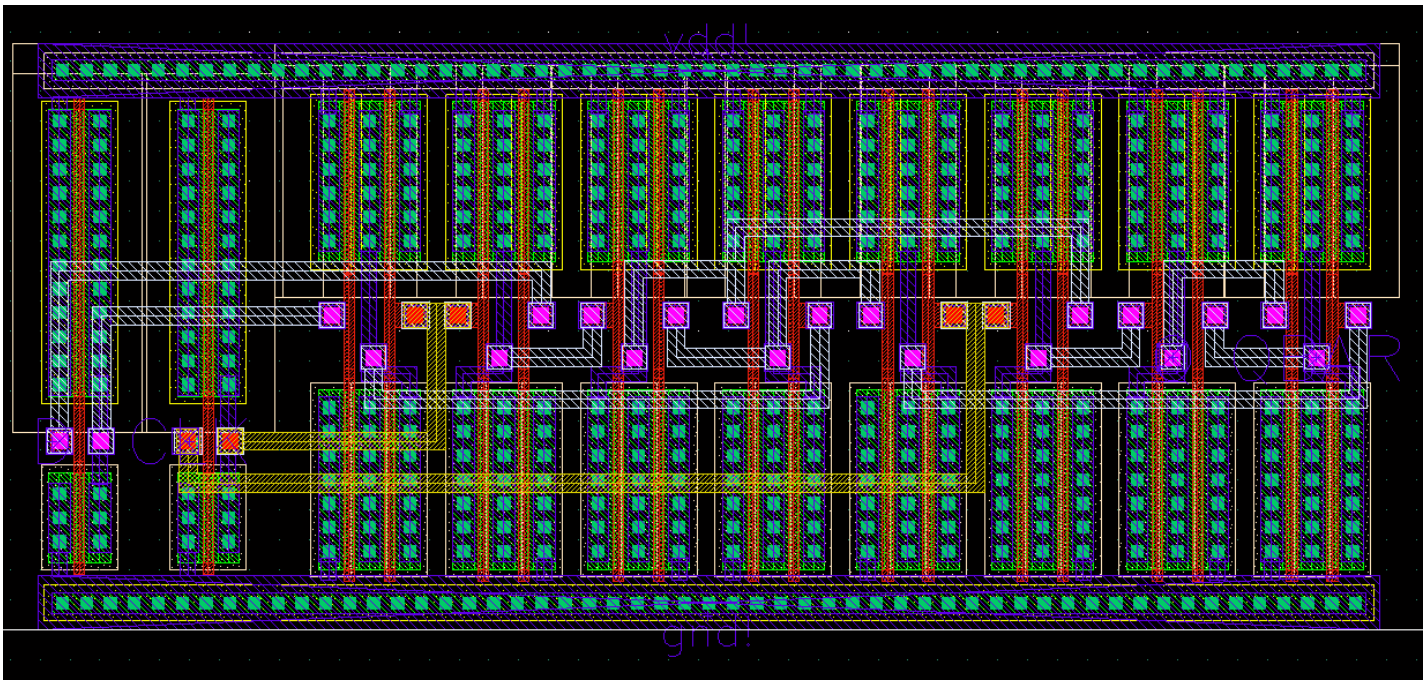


Figure 8: Layout View of D Flip-Flop

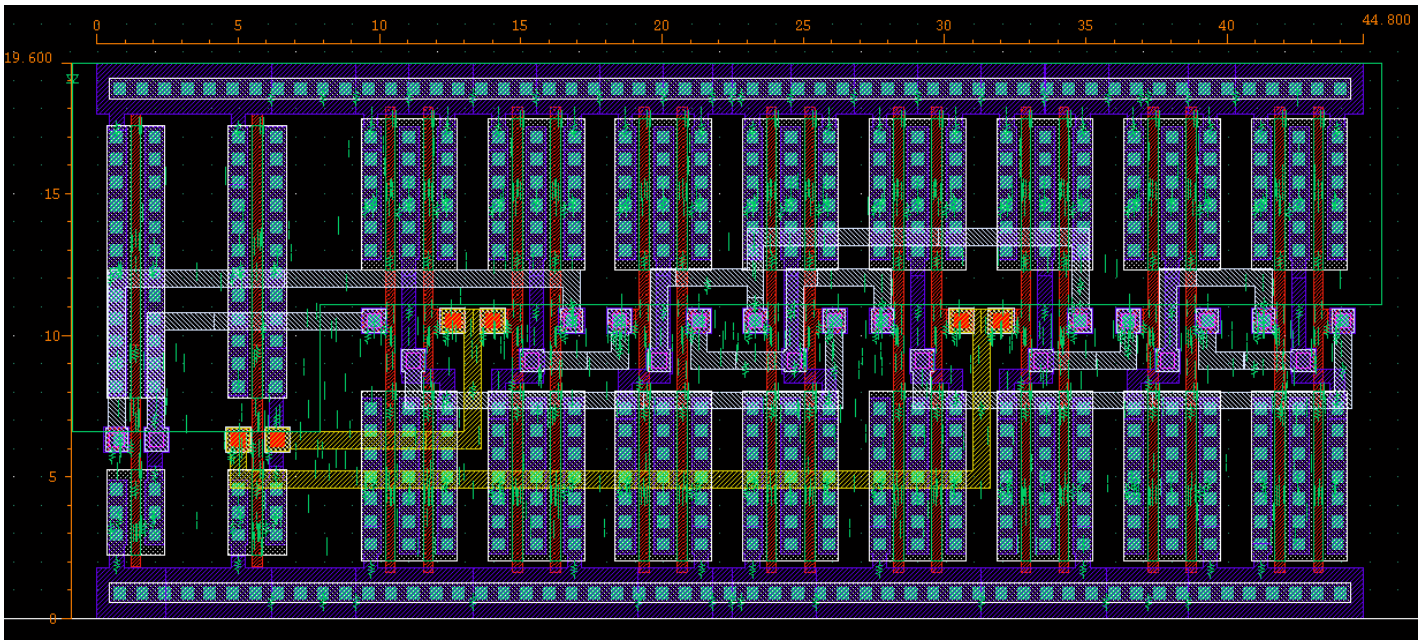


Figure 9: Extracted View of D Flip-Flop

Total layout area is 19.6 x 44.8 μm^2, which are both multiples of 1.4 µm. MET3 layer is used for clock distribution while MET2 layer is used for other interconnections. Fig.9 shows the layout after RC extraction. As we will observe after post-layout simulations, maximum parasitic capacitances are 27.15 fF and 22.72 fF shown in VDD and GND nets respectively.

Below Fig.10 and Fig.11 shows the details about input and output pins which are important in terms of Standard Cell Layout rules. Measurements are performed by choosing the only visible layer as PIN-M1.

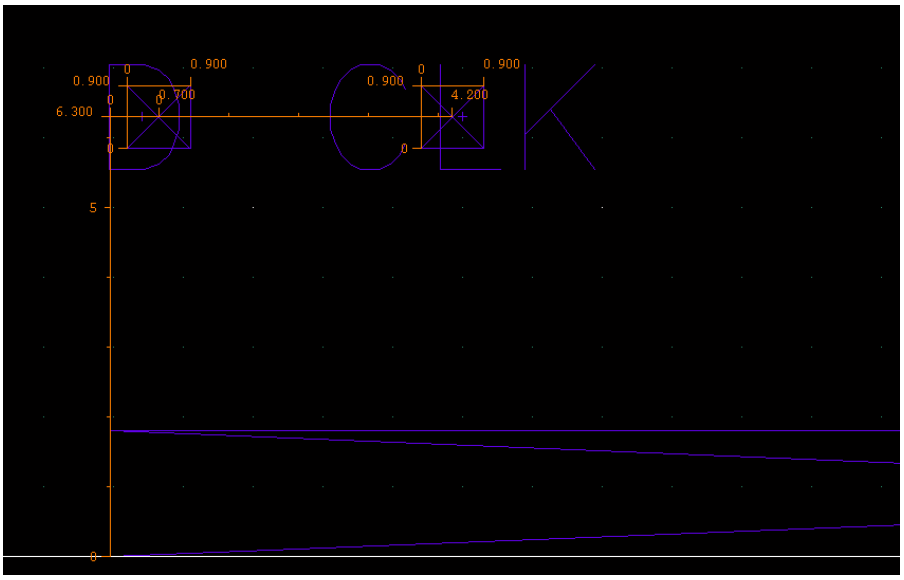


Figure 10: Dimensions and Placing of Input Pins

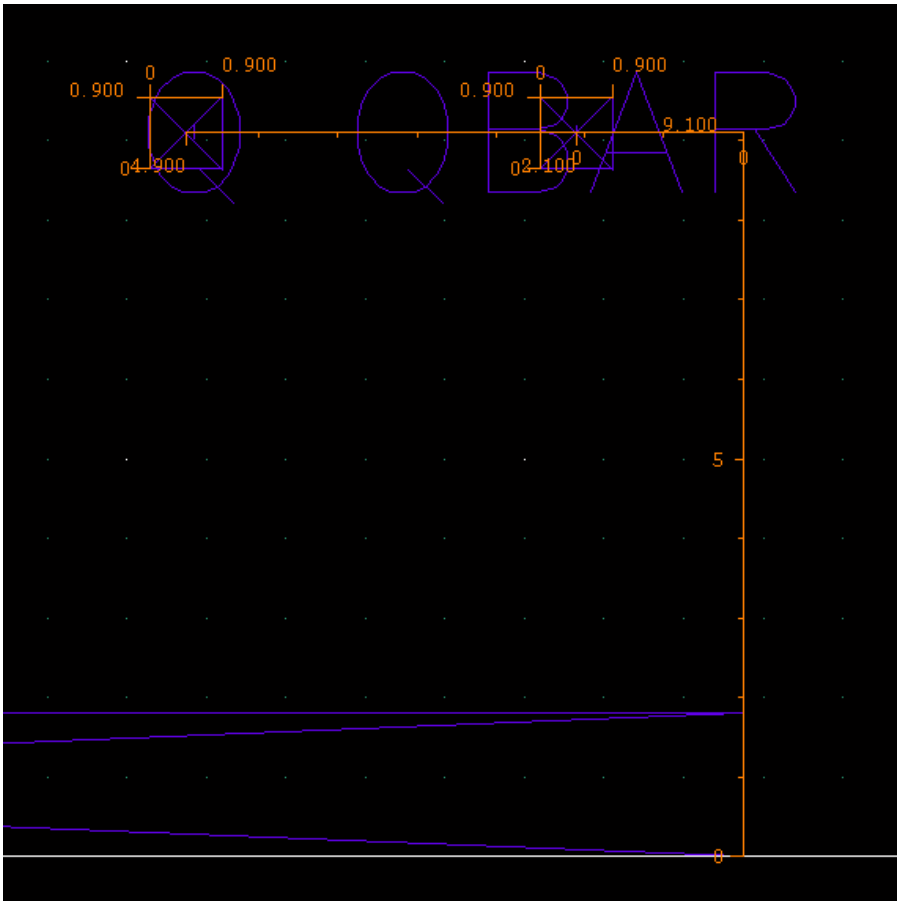


Figure 11: Dimension and Placing of Output Pins

4. SCHEMATIC SIMULATION RESULTS:

To make simulations for D flip-flop, we used the circuitry shown in Fig.12. As specified in introduction, output load is a 50 fF capacitor. Frequency of the clock signal is chosen as 1 GHz, with 100 ps rise and fall times and 50% duty cycle. We supplied square wave to input D with 2 ns period so as to see both high-to-low and low-to-high transition in as much small time period as possible.

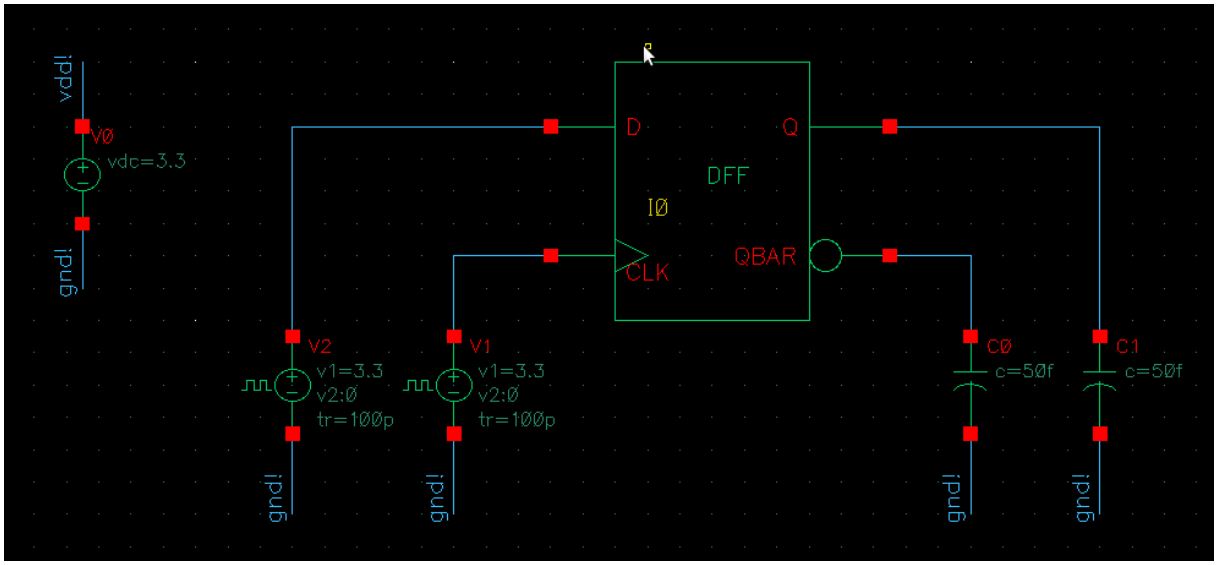


Figure 12: Simulation Circuitry for D Flip-Flop

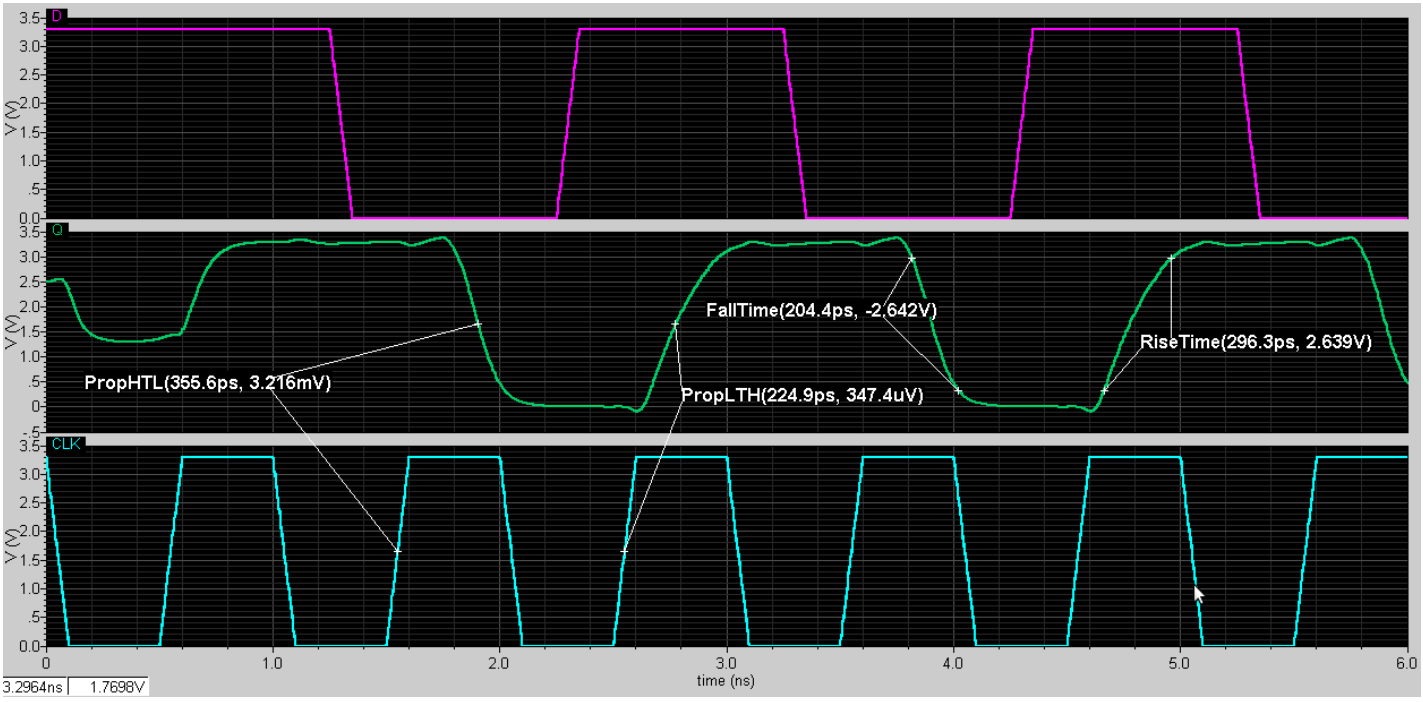


Figure 13: Schematic Simulation – Timing Results

Fig.13. shows the schematic simulation results. Propagation time delay for high-to-low transition is 355.6 ps, for low-to-high transition it is 224.9 ps. Propagation time delays are measured from the point when clock signal comes to 50% value (1.65 V) to the point when output (Q) comes to its 50% value (1.65 V). Rise and fall times are measured between the 10% (0.33 V) and 90% (2.97 V) values of the output signal. Fall time is measured as 204.4 ps while rise time measured as 296.3 ps.

Observe that $\tau_{low\text{-}to\text{-}high} < \tau_{low\text{-}to\text{-}high}$ and $t_{fall} < t_{rise}$.

As important as timing results, Fig.13 also shows the stable behavior of the D flip-flop. As can be seen, there is not a settling problem at the output of the flip-flop.

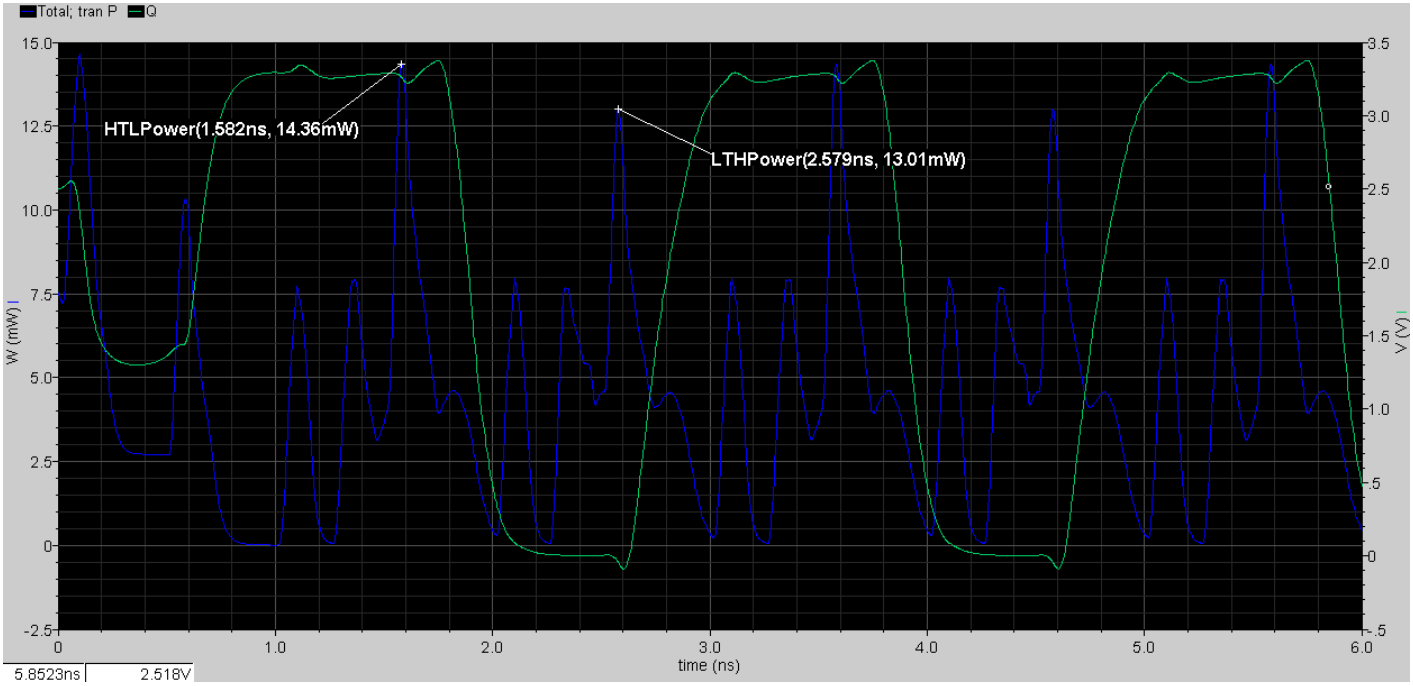


Figure 14: Schematic Simulation – Power Consumption Results

Fig.14 shows the power consumption results of D flip flop after schematic simulations. As can be seen, power consumption values peak at the start of the transitions. While output stays constant, power consumption values are considerably low.

Peak power consumption for high-to-low transition is 14.36 mW, while 13.01 mW for low-to-high transition. Another metric to measure power consumption is rms value of the total power consumed. In our case, rms power is measured as 5.72 mW.

Observe that peak powers, $P_{low\text{-}to\text{-}high} < P_{high\text{-}to\text{-}low}$

5. POST LAYOUT SIMULATION RESULTS:

Same circuitry (Fig.12) is used for post-layout simulations. In post-layout simulations, RC extracted view of the layout is used to get more realistic simulation results.

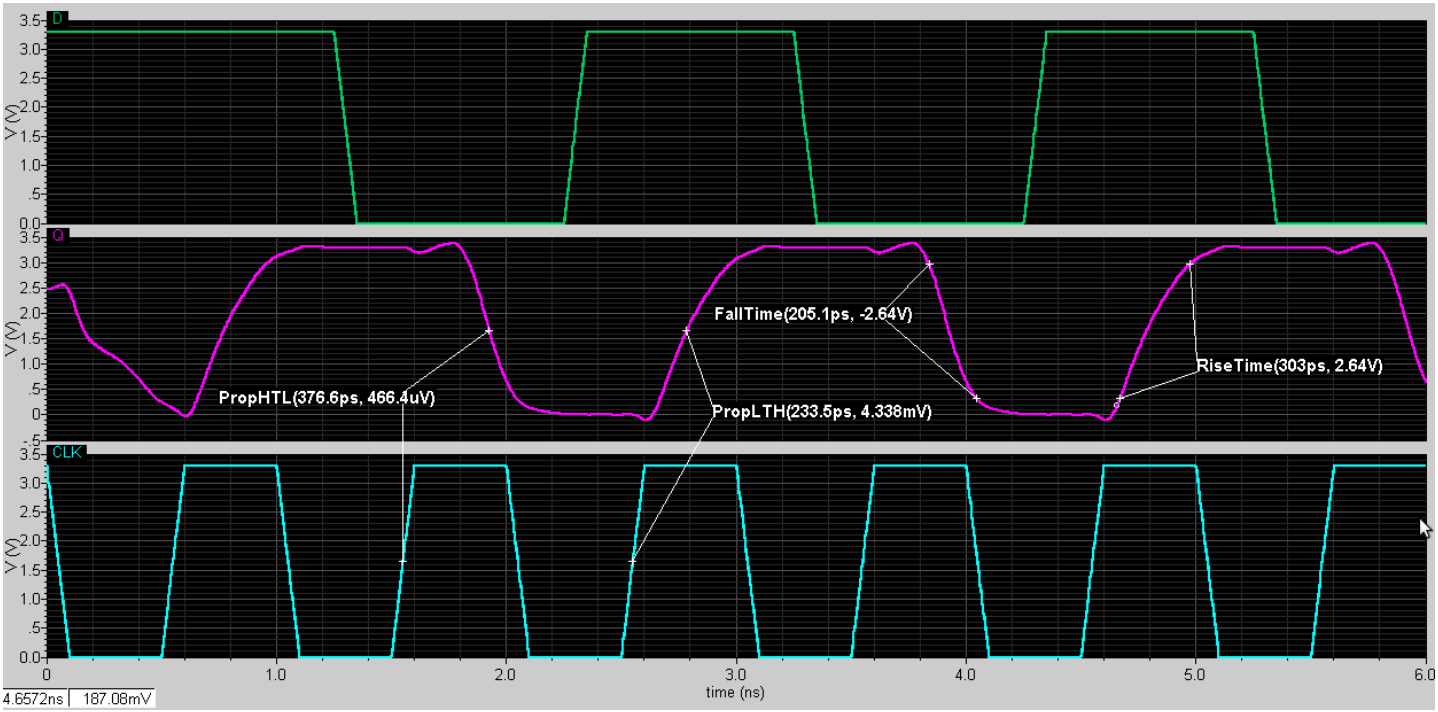


Figure 15: Post-Layout Simulations – Timing Results

After post-layout simulations propagations time delays are measured as follows: propagation high-to-low is 376.6 ps, propagation low-to-high is 233.5 ps. Fall time is measured as 205.1 ps while rise time is 303 ps.

Observe that in post-layout simulation, all timing values are larger than schematic simulation.

Again observe that, still $\tau_{low\text{-}to\text{-}high} < \tau_{low\text{-}to\text{-}high}$ and $t_{fall} < t_{rise}$.

Below Fig.16 shows the power consumption behavior of the D flip-flop. As you can see the behavior is quite similar with values high-to-low peak power consumption of 15 mW, low-to-high peak power consumption of 13.99 mW and rms power of 6.062 mW.

Again we have, $P_{low\text{-}to\text{-}high} < P_{high\text{-}to\text{-}low}$.

As you see, all power consumption values are larger in post-layout simulations.

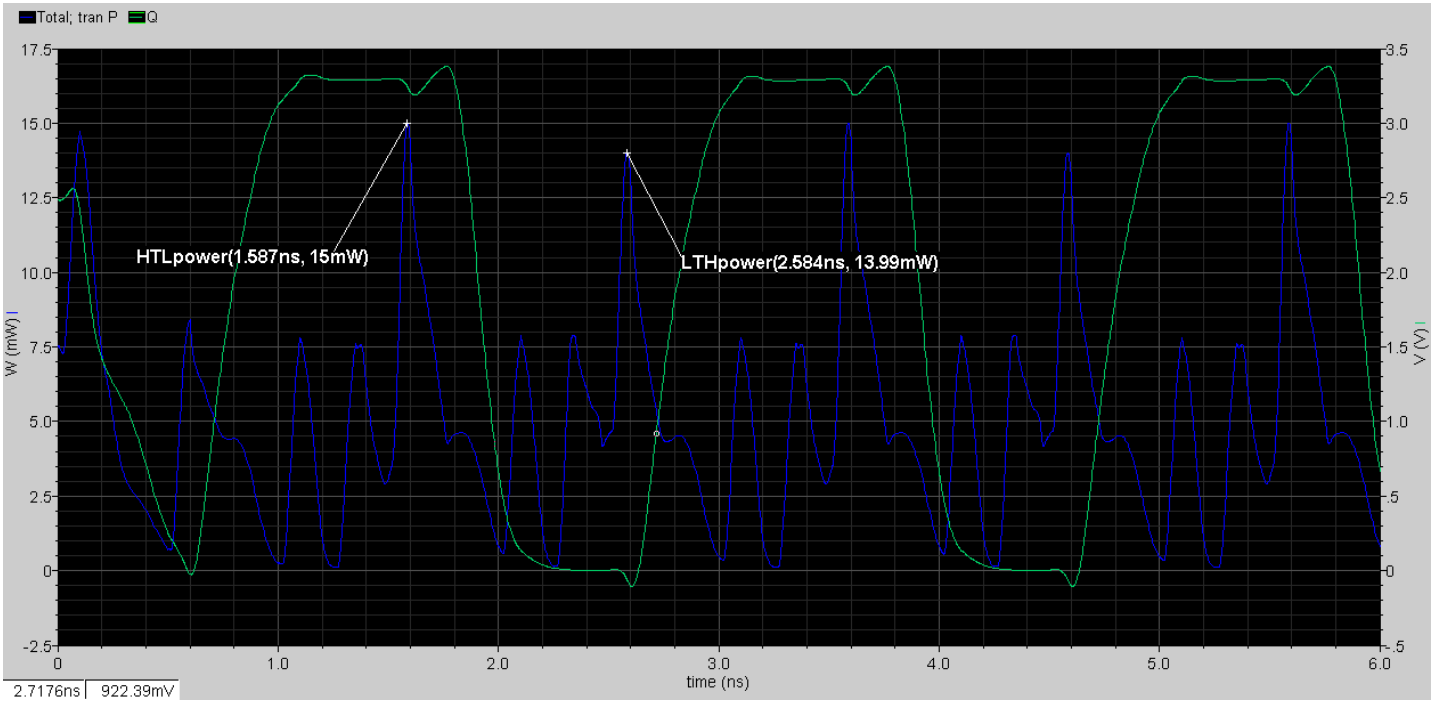


Figure 16: Post-Layout Simulations – Power Consumption Results

All Parasitics for DFF

Close | Save... | Help

Report: decoupled C ■ coupled C

NetName	R	sum C
/gnd!	NA	27.15f
/vdd!	NA	22.72f
/net27	NA	10.67f
/CLK	NA	10.61f
/net30	NA	9.344f
/net6	NA	8.811f
/D	NA	8.052f
/net11	NA	8.044f
/net26	NA	7.759f
/Q	NA	6.243f
/net23	NA	6.141f
/net14	NA	6.088f
/QBAR	NA	5.954f
/net8	NA	5.879f
/I11/net15	NA	1.344f
/I4/net15	NA	1.326f
/I9/net15	NA	1.322f
/I2/net15	NA	1.302f
/I0/net15	NA	1.291f
/I15/net15	NA	1.29f
/I14/net15	NA	1.27f
/I7/net15	NA	1.262f

Number of parasitic instances R: 270 C: 856 L: 0

Figure 17: Parasitic Capacitances of D Flip-Flop

Fig.17 on the left shows the parasitic capacitances found in the design after RC extraction. As you can see, maximum capacitances seen at any node is 27.15 fF and 22.72 fF, seen at VDD and GND nodes. Since VDD and GND nodes include huge MET1 rails, it is normal to see such large capacitance at these nodes.

If you look at the parasitic capacitances seen at output nodes they are 6.243 fF for Q and 5.954 fF for QBAR output, which reasonably small parasitic values. So we can state that layout of the design is acceptable.

6. OVERALL DISCUSSION and CONCLUSION:

Below Table.1 shows the all simulation results, and includes a comparison between schematic simulations and post-layout simulations. As you can see, worst timing result is propagation delay high-to-low, 376.6 ps, which is much smaller than the clock frequency. Thus we can conclude that our design works properly at 1 GHz. (By looking at simulation results, our D Flip-Flop can even work at 2.5 GHz! – 376.6 ps x 2.5 GHz = 0.9415 < 1)

	Schematic Simulation	Post-Layout Simulation
$\tau_{prop,\ low\text{-}to\text{-}high}$	224.9 ps	233.5 ps
$\tau_{prop,\ high\text{-}to\text{-}low}$	355.6 ps	376.6 ps
t_{rise}	296.3 ps	303 ps
t_{fall}	204.4 ps	205.1 ps
$PeakPower_{low\text{-}to\text{-}high}$	13.01 mW	13.99 mW
$PeakPower_{high\text{-}to\text{-}low}$	14.36 mW	15 mW
rms power	5.752 mW	6.062 mW

Table 1: Overall Simulation Results

In overall, our D Flip-Flop works properly and in very fast manner. The trade-off for this is high power consumption. For better performance, a super buffer can be added to the output of the D flip-flop to further decrease rise and fall times. If the use of MET3 layer is not possible, then other topologies should be used.

VDD	$V_{T0,n}$	$V_{T0,p}$	$\mu_n C_{OX}$	$\mu_p C_{OX}$
3.3 V	0.55 V	0.62 V	160 $\mu A/V^2$	56.7 $\mu A/V^2$

Table 2: AMS 0.35u design parameters